ABSTRACT

An output port for an integrated circuit includes a bandwidth manager for assisting in the off-loading of internal state data during debug periods. The bandwidth manager operates to take internal state data at its normal frequency, and outputs at least the most important portions of that data to external logic. During periods when the output port is able to keep up with the internal sources being sampled, the bandwidth manager will cause all of the state data to be transmitted. If the output port becomes saturated, the bandwidth manager will select the most important portions of the internal state data to be transmitted off –chip, and will drop the less important information. The bandwidth manager is configured to operate dynamically based on the ability of the output port to keep up with the data being generated by the internal sources. The bandwidth manager determines the importance of data based on principles underlying the structure of packets, rather than on detailed parsing of packets, and without relying on knowledge of packet semantics.